PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : H04J 3/14, H04L 12/26 — A1

(11) International Publication Number: WO 94/13073

(43) International Publication Date: 9 June 1994 (09.06.94)

(21) International Application Number: PCT/FI93/00519

(22) International Filing Date: 2 December 1993 (02.12.93)

(30) Priority Data:
925481 2 December 1992 (02.12.92) FI

(71) Applicant *(for all designated States except US)*: NOKIA TELECOMMUNICATIONS OY [FI/FI]; Mäkkylän puistotie 1, FIN-02600 Espoo (FI).

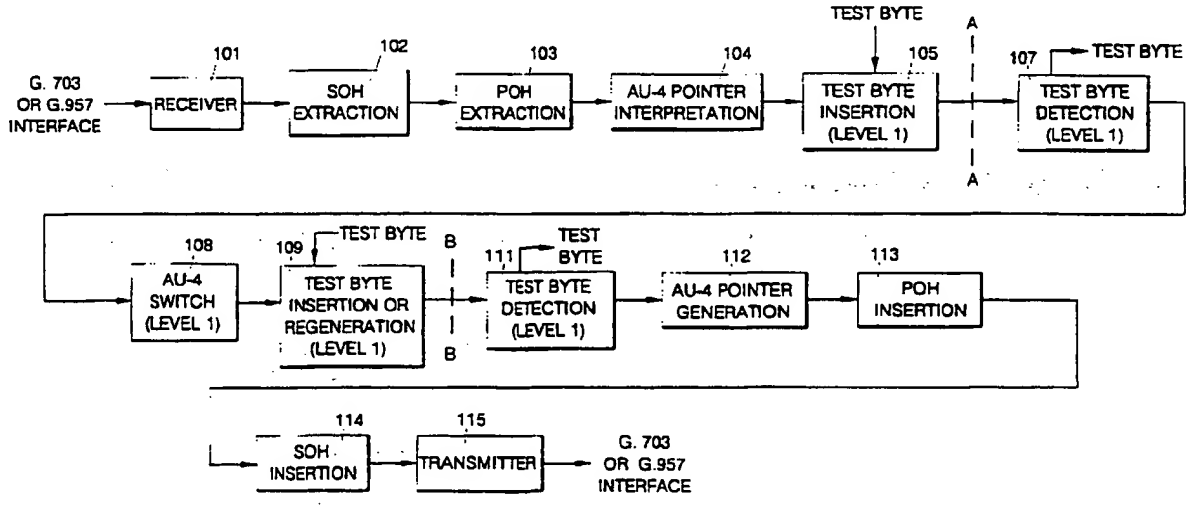
(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: KLINE, Eric [US/US]; 42 Knollwood Drive, Deptford, NJ 08096 (US). KIVIMANNILA, Arvi [FI/FI]; Ellipsikuja 3 D 26, FIN-02210 Espoo (FI). SUVITAIVAL, Pekka [FI/FI]; Ruotsinkyläntie 95, FIN-01590 Maisala (FI).

(74) Agent: OY KOLSTER AB; Iso Roobertinkatu 23, P.O. Box 148, FIN-00121 Helsinki (FI).

(81) Designated States: AU, DE, GB, JP, SE, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
In English translation (filed in Finnish).

(54) Title: A METHOD FOR TESTING A NETWORK ELEMENT IN A SYNCHRONOUS DIGITAL TELECOMMUNICATION SYSTEM



(57) Abstract

The invention relates to a method for testing the condition of a network element in a synchronous digital telecommunication system, such as the SDH or SONET system, which signal has a frame structure consisting of a predetermined number of bytes fixed in length and containing a pointer indicating the phase of payload within the frame structure. In order that the condition of the network element could be tested within the network element, a test byte (AUT, TUT) is inserted (105, 109) within the network element in at least one predetermined location in the frame structure, and said test byte is read (107, 111) within the network element at least at one monitoring point positioned after the insertion point.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**GB**	United Kingdom	**MR**	Mauritania
AU	Australia	**GE**	Georgia	**MW**	Malawi
BB	Barbados	**GN**	Guinea	**NE**	Niger
BE	Belgium	**GR**	Greece	**NL**	Netherlands
BF	Burkina Faso	**HU**	Hungary	**NO**	Norway
BG	Bulgaria	**IE**	Ireland	**NZ**	New Zealand
BJ	Benin	**IT**	Italy	**PL**	Poland
BR	Brazil	**JP**	Japan	**PT**	Portugal
BY	Belarus	**KE**	Kenya	**RO**	Romania
CA	Canada	**KG**	Kyrgystan	**RU**	Russian Federation
CF	Central African Republic	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CG	Congo			**SE**	Sweden
CH	Switzerland	**KR**	Republic of Korea	**SI**	Slovenia
CI	Côte d'Ivoire	**KZ**	Kazakhstan	**SK**	Slovakia
CM	Cameroon	**LI**	Liechtenstein	**SN**	Senegal
CN	China	**LK**	Sri Lanka	**TD**	Chad
CS	Czechoslovakia	**LU**	Luxembourg	**TG**	Togo
CZ	Czech Republic	**LV**	Latvia	**TJ**	Tajikistan
DE	Germany	**MC**	Monaco	**TT**	Trinidad and Tobago
DK	Denmark	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**US**	United States of America
FI	Finland	**ML**	Mali	**UZ**	Uzbekistan
FR	France	**MN**	Mongolia	**VN**	Viet Nam
GA	Gabon				

A method for testing a network element in a synchronous digital telecommunication system

The invention relates to a method according to the preamble portion of the accompanying claim 1 for testing a network element in a synchronous digital telecommunication system. As used herein the network element refers to a network element defined in the CCITT recommendations, which may be e.g. a Terminal Multiplexer, a Digital Cross-Connect System, an Add/Drop multiplexer or regenerator.

The current digital transmission network is plesiochronous, that is, each 2-Mbit/s basic multiplex system has a dedicated clock independent of other systems. It is therefore impossible to locate a single 2-Mbit/s signal in the bit stream of a higher-order system, but the higher-level signal has to be de-multiplexed through each intermediate level down to the 2 Mbit/s level to extract the 2-Mbit/s signal. For this reason, especially the construction of branch connections requiring several multiplexers and de-multiplexers has been expensive. Another disadvantage of the plesiochronous transmission network is that equipments from two different manufacturers are not usually compatible.

The above drawbacks, among other things, have led to the specification of the new synchronous digital hierarchy SDH. It is specified in the CCITT recommendations G.707...G.709 and G.781...G784. The synchronous digital hierarchy is based on STM-N transfer frames (Synchronous Transport Modules) located on several levels of hierarchy N (N = 1, 4, 16...). Existing PCM systems, such as 2-, 8- and 34-Mbit/s systems are multiplexed into a synchronous 155.520-Mbit/s frame of the lowest level of the SDH

(N=1); consistently with the above, this frame is called the STM-1 frame. On the higher levels of hierarchy the bit rates are multiples of the bit rate of the lowest level. In principle, all nodes in a synchronous transmission network are synchronized to a single clock. If some of the nodes should, however, lose connection to the common clock, problems would arise in the internodal connections. It is also necessary that the phase of the frame can be determined easily at the reception. The above-mentioned matters have led to the introduction of a pointer in the SDH telecommunications. The pointer is a number indicating the phase of the payload within the frame, i.e. the pointer points to a byte in the STM frame from which the payload begins.

Figure 1 illustrates the structure of the STM-N frame, and Figure 2 illustrates a single STM-1 frame. The STM-N frame comprises a matrix with 9 rows and N x 270 columns so that there is one byte at the junction between each row and the column. Rows 1-3 and rows 5-9 of the N x 9 first columns comprise a section overhead SOH, and the row 4 comprises an AU pointer. The rest of the frame structure is formed of a section having the length of N x 261 columns and containing the payload section of the STM-N frame.

Figure 2 illustrates a single STM-1 frame which has rows 270 bytes in length, as described above. The payload section comprises one or more administration units AU. In the specific case shown in the figure, the payload section consists of the administration unit AU-4, into which a virtual container VC-4 is inserted. (Alternatively, the STM-1 transfer frame may contain three AU-3 units each containing a corresponding virtual container VC-3). The VC-4 in turn consists of a path overhead POH located at the beginning of

each row and having the length of one byte (9 bytes altogether), and of the payload section in which there are lower-level frames also comprising bytes allowing interface justification to be performed in connection with mapping when the rate of the information signal to be mapped deviates from its nominal value to some extent. (Mapping of the information signal into the STM-1 frame is described e.g. in the patent applications AU-B-34689/89 and FI-914746.)

Each byte in the AU-4 unit has its own location number. The above-mentioned AU pointer contains the location of the first byte of the VC-4 container in the AU-4 unit. The pointers allow positive or negative pointer justifications to be performed at different points in the SDH network. If a virtual container having a certain clock frequency is applied to a network node operating at a clock frequency lower than the above-mentioned clock frequency of the virtual container, the data buffer will be filled up. This requires negative justification: one byte is transferred from the received virtual container into the overhead section of the frame to be transmitted, while the pointer value is decreased by one. If the rate of the received virtual container is lower than the clock rate of the node, the data buffer tends to be emptied, which calls for positive justification: a stuff byte is added to the received virtual container and the pointer value is incremented by one.

Figure 3 shows how the STM-N frame can be formed of existing bit streams. These bit streams (1.5, 2, 6, 8, 34, 45 or 140 Mbit/s, shown in the right in the figure) are packed at the first stage into containers C specified by CCITT. At the second stage, overhead bytes containing control data are inserted into the containers, thus obtaining the above-described virtual

container VC-11, VC-12, VC-2, VC-3 or VC-4 (the first suffix in the abbreviations represents the level of hierarchy and the second suffix represents the bit rate). This virtual container remains intact while it passes through the synchronous network up to its point of delivery. Depending on the level of hierarchy, the virtual containers are further formed either into so-called tributary units TU or into AU units (AU-3 and AU-4) already mentioned above by providing them with pointers. The AU unit can be mapped directly into the STM-1 frame, whereas the TU units have to be assembled through tributary unit groups TUG and VC-3 and VC-4 units to form AU units which then can be mapped into the STM-1 frame. In Figure 3, the mapping is indicated by a continuous thin line, the aligning with a broken line, and the multiplexing with a continuous thicker line.

As is to be seen from Figure 3, the STM-1 frame may be assembled in a number of alternative ways, and the content of the highest-level virtual container VC-4, for instance, may vary, depending on the level from which the assembly has been started and in which way the assembly has been performed. The STM-1 signal may thus contain e.g. 3 TU-3 units or 21 TU-2 units or 63 TU-12 units or a combination of the units mentioned. As the higher-level unit contains several lower-level units, e.g. the VC-4 unit contains TU-12 units (there are 63 such units in a single VC-4 unit, cf. Figure 3), the lower-level units are mapped into the higher-level frame by interleaving so that the first bytes are first taken consecutively from each one of the lower-level units, then the second bytes, etc. It is shown in the example of Figure 2 how the VC-4 unit contains first the first bytes of the 63 TU-12 unit successively, then the second bytes of all 63 TU-12

units, etc.

The above-described SDH frame structures and the assembly of such structures have been described e.g. in References [1] and [2], which are referred to for a more detailed description (the references are listed at the end of the specification).

Network management is also included in the above-mentioned CCITT specifications of the SDH (network management was not taken into account in the specifications of the plesiochronous network). For this purpose, the frame structure has the above-described overhead areas (section overhead and path overhead, SOH, POH), which allow the introduction of network management channels. The management channels formed by bytes in these overhead areas and the use of the channels are specified in the CCITT recommendation G.784. The specification of the functions of the overhead area aims at the creation of open network management systems.

The CCITT recommendations, however, concern only the monitoring of network failures (they may be used e.g. to detect a cable break caused by an excavator). The remaining problem is the testing of the internal condition of an individual network element, such as the testing of the busses and connections of a network element. No specifications have been issued for the internal testing of network elements.

The object of the present invention is to provide a method suitable for testing the internal operation of a network element, which allows the search for internal failures in a network element and the testing of the internal performance of the network element. This is achieved by a method according to the invention which is characterized by what is disclosed in the characterizing portion of the accompanying

claim 1.

The invention is based on the idea that at least one test byte is inserted in the frame structure within the network element and the test byte is then monitored at one or more monitoring points so as to locate a failed or inappropriately operating point.

The solution according to the invention allows the testing of the condition of a network element and the search for failure situations in a manner such that the normal propagation of the payload signal is not disturbed at all. As the method according to the invention monitors the internal failures and switching states of the network element, all (inbound and outbound) cables can be detached from the network element while nevertheless continuing the testing procedure according to the invention.

A single frame may contain a plurality of test bytes which may be on different levels of hierarchy so that they can be used for testing the condition of different functions (such as time and space switching). The content of the test byte may also change at predetermined intervals so that the test bytes form a predetermined sequence repeated in the same format. It is also possible to shift the test byte insertion and/or monitoring point continuously within the network element in order to locate a detected failure or other deficiency with sufficient accuracy.

It is preferable to extract the test bytes before the output interface of the network element in order that the corresponding locations in the frame structure could be used for other purposes.

In the following the invention will be described more closely, still referring to Figures 4 to 6, by means of the examples shown in the attached drawings, in which

Figure 1 illustrates the basic structure of a single STM-N frame;

Figure 2 illustrates the structure of a single STM-1 frame;

Figure 3 illustrates the assembly of the STM-N frame from existing PCM systems;

Figure 4 illustrates the principle according to the invention in an AU-4 cross-connect unit;

Figure 5 shows one preferred test byte location;

Figure 6 shows another preferred test byte location when the testing takes place on a level of hierarchy lower than above.

Figure 4 shows the principle of the method according to the invention in an AU-4 cross-connect unit where STM-1 payload signals are cross-connected. A STM-1 signal is received at a receiver 101 in the cross-connect unit from an interface complying with the CCITT recommendations G.703 or G.957. The section overhead SOH and the path overhead POH are first extracted from the received signal in units 102 and 103, respectively. The signal frequency is not changed, and so the empty space can be used for inserting one or more test bytes in accordance with the invention.

After the extraction of the section and path overheads, the signal is applied to an AU-4 pointer interpretation unit 104, where the AU-4 pointer is interpreted in compliance with the CCITT recommendations (Reference [1]). After the pointer interpretation the signal is applied to a first insertion unit 105, where a test byte of the first level of hierarchy (in this specific case the AU-4 level) is inserted into the frame structure at a predetermined location. (Figure 5 to be described below shows one possible insertion location in the frame). The test byte to be

inserted into each particular frame is obtained from a processor (not shown). From the insertion unit 105 the signal is applied through an intersection A-A (e.g. a bus) to a first detection unit 107 for the test byte of the first level of hierarchy so as to read the test byte from each frame and to transfer the read byte to the above-mentioned processor, which compares the read test byte sequence with the inserted test byte sequence. As a result of the comparison, information is obtained about the condition of the network element between the insertion and detection units 105 and 107.

From the detection unit 107 the signal is applied to an AU-4 switch, which performs the switching of the STM-1 payload signal in space. From the switch 108 the signal is applied to a second insertion unit 109, where the processor again inserts a predetermined test byte sequence (which may be different from the first inserted sequence and have a different location in the frame structure). The regeneration of the previously inserted test bytes may also be performed in the unit 109. From the second insertion unit 109 the signal is applied through an intersection B-B (e.g. a bus) to a second detection unit 111, where the test bytes are read (and extracted) from each frame and the read bytes are transferred to the above-mentioned processor, which again compares the read test byte sequence at least with the previously inserted test byte sequence. If the second test byte sequence was inserted into the frame structure at a different location than the first one, it is possible to monitor both of the test byte sequences in the second detection unit; for instance, the first one can be used for testing the switching and the second one for testing the intersection B-B. At this stage, as the detection unit 111 is the last point of detection

of the test byte within the network element, it is preferable to remove the test bytes entirely from the signal in order that the test byte locations could be subsequently used for other purposes.

After the extraction of the test byte(s) from the frame structure, a new AU-4 pointer is generated in a generation unit 112. New path and section overheads are then inserted in the signal in units 113 and 114, respectively, whereafter the complete STM frame is again applied through a transmitter 115 complying with G.703 or G.957 and further to the SDH network.

Figure 4 is a functional block diagram of the cross-connect unit. In practice, the arrows between the blocks may represent e.g. signal lines on printed circuit boards, cables, backplane buses or other conductors, which may extend between racks, subrack boards or integrated circuits. Even though the test bytes were inserted on a single level of hierarchy in Figure 4 (level 1 in the figure), it is also possible to insert test bytes on other levels of hierarchy, as will be described below referring to Figure 6.

Figure 5 shows the section overhead SOH of the STM-1 frame and one preferred test byte location when the testing takes place on the AU-4 level as shown in Figure 4. The section overhead contains a Regenerator Section Overhead RSOH, which consists of the first three rows, and a Multiplexer Section Overhead MSOH, which consists of the four lowest rows. The former is assembled and disassembled by the regenerator functions, and the latter at the points of assembly and disassembly of AUG units (cf. Figure 3). In the section overhead, e.g. the bits D1-D12 form the 192 kbit/s and 576 kbit/s channels intended for network management. The bytes B1 and B2 are intended for monitoring the line error rate. However, these prior

art methods are not able to detect the internal failures of a network element.

The test byte AUT according to the present invention is inserted in this specific case as the ninth byte of the second row of the section overhead (SOH). Normally, this byte is reserved for national use. It is preferable to use bytes reserved for national use as test byte locations because it is improbable that they would subsequently be needed for a purpose which would prevent their use as test byte locations.

Figure 6 shows another preferred test byte location. In this case the test byte is intended for testing taking place on the TU-12 level (e.g. for testing the time switching in the case shown in Figure 2, where the AU-4 unit contains 63 TU-12 channels). The TU test byte TUT is inserted in the TU-12 frame at the location of the V4 byte. The TU-12 frame is 500 µs in length, thus corresponding to four STM-1 frames, and the V4 byte is a byte which begins the fourth STM-1 frame in the four-frame multiframe formed by the TU-12 frame. In Figure 6, the data bytes contained in the TU-12 frame are indicated with the numerals 0...139. The test byte is inserted in the first byte of the VC-12 in the fourth frame.

Even though two preferred test byte locations have been described above, it is possible in principle to insert the test byte in the frame structure at any empty location (e.g. a location where no payload signal propagates or a location for which no use is specified in the recommendations). The location also depends on how the STM-1 frame has been assembled (cf. Figure 3). The above examples also apply in a case where the VC-4 unit contains 63 TU-12 units. In addition to the above-mentioned bytes reserved for

national use, possible test byte insertion locations include empty and unused bytes in the frame structure, empty pointer bytes and reserved bytes.

The method according to the invention thus allows a failure or some other functional deficiency to be located between a monitoring point and a test byte insertion location or a preceding monitoring point, respectively. By shifting the insertion and/or monitoring point, the failure can be located accurately. In some cases, it is possible to judge the type of the failure from the format of the received test byte or test byte sequence; for example, in testing a bus where bits propagate in parallel, it is possible to judge that a bus wire has failed from a bit inappropriately received. Also, it is possible to locate e.g. a solder bridge if it is detected that the error is also reflected in an adjacent bit.

The test byte to be written into the frame at a predetermined location can be changed at regular intervals so that the test bytes form a predetermined sequence. One such sequence may consist of four test bytes as follows: 11111111, 10101010, 01010101, 00000000. The same test byte sequence may be inserted several times, and it may be detected several times. Failures in integrated circuits may be mapped out e.g. by monitoring whether the errors occur only in zeros or only in ones, respectively. The frequency of changing the test byte may also be slow with respect to the frame rate. It is often advantageous to use different test byte sequences for different purposes; for example, in testing a bus to check the condition of each bus conductor, it is advisable to use a sequence different from that used for testing the switching, where the path of propagation of a signal through a switch is monitored. The method according to the

invention can be used advantageously e.g. for testing the switching state of a cross-connect unit, as the test byte undergoes the same switching as the actual signal.

Even though the invention has been described above with reference to the examples of the attached drawings, it is obvious that the invention is not limited to them, but it can be modified in many ways within the inventive idea disclosed above and in the accompanying claims. The practical, more detailed application may thus vary, depending on the network element and the internal part of the network element to be tested.

References:

[1] CCITT *Blue Book*, Recommendation G.709: "Synchronous Multiplexing Structure", May 1990.

[2] SDH - Ny digital hierarki, TELE 2/90.

[3] CCITT *Blue Book*, Recommendation G.783: "Characteristics of Synchronous Digital Hierarchy (SDH) Multiplexing Equipment Functional Blocks", August 1990, Annex B.

Claims:

1. Method for testing the condition of a network element in a synchronous digital telecommunication system, such as the SDH or SONET system, which signal has a frame structure consisting of a predetermined number of bytes fixed in length and containing a pointer indicating the phase of payload within the frame structure, c h a r a c t e r i z e d in that a test byte (AUT, TUT) is inserted (105, 109) within the network element in at least one predetermined location in the frame structure, and said test byte is read (107, 111) within the network element at least at one monitoring point positioned after the insertion point for testing the condition or state of the network element.

2. Method according to claim 1, c h a r a c t e r i z e d in that said at least one test byte is inserted in a frame structure overhead area (SOH, POH).

3. Method according to claim 1, c h a r a c t e r i z e d in that a plurality of test bytes (AUT, TUT) are inserted on different levels of hierarchy in the frame structure.

4. Method according to claim 1, c h a r a c t e r i z e d in that the test byte monitoring point is shifted within the network element to locate a failure more precisely.

5. Method according to claim 1, c h a r a c t e r i z e d in that the test byte insertion point is shifted within the network element to locate a failure more precisely.

6. Method according to claim 1, c h a r a c t e r i z e d in that the test bytes are removed before the output interface of the network element.

7. Method according to claim 1, c h a r a c t e r i z e d in that the content of the test byte is changed at regular intervals.

8. Method according to claim 7, c h a r a c t e r i z e d in that the test byte is changed at regular intervals in a manner such that the test bytes form a predetermined sequence repeated in the same format.

9. Method according to claim 8, c h a r a c t e r i z e d in that the frequency of changing of the test byte is slower than the frame rate.

10. Use of the method according to claim 1 for testing the switching state of a cross-connect unit by monitoring the propagation path of a signal through a switch.

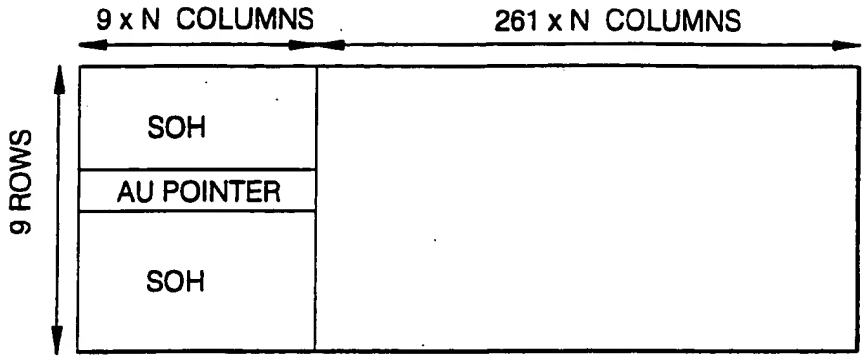


FIG. 1

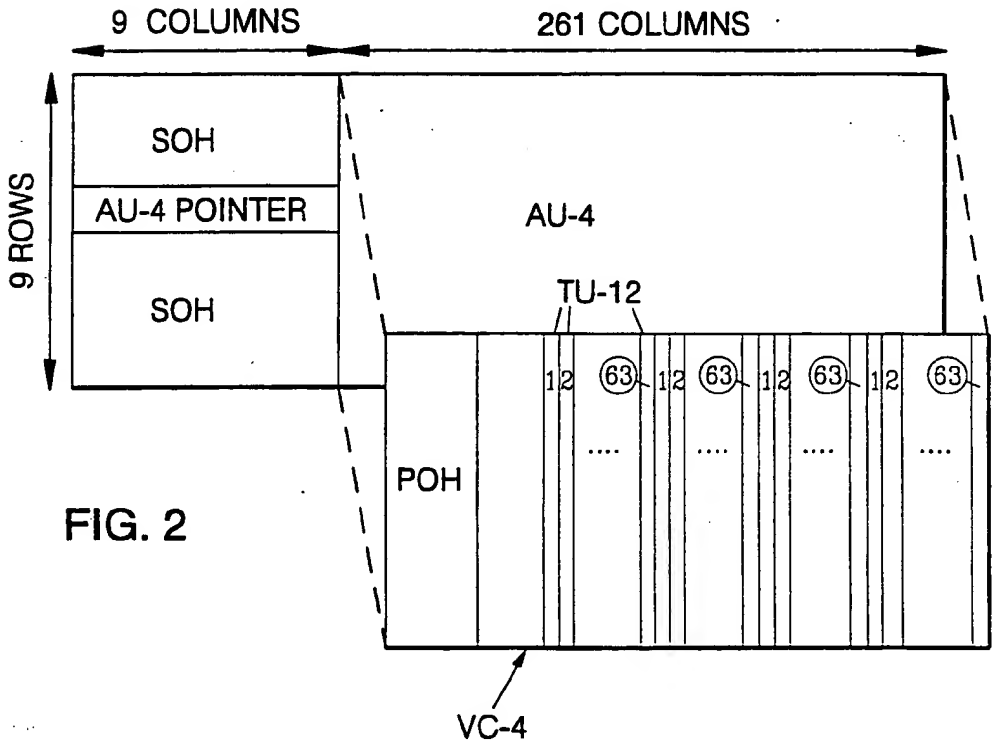


FIG. 2

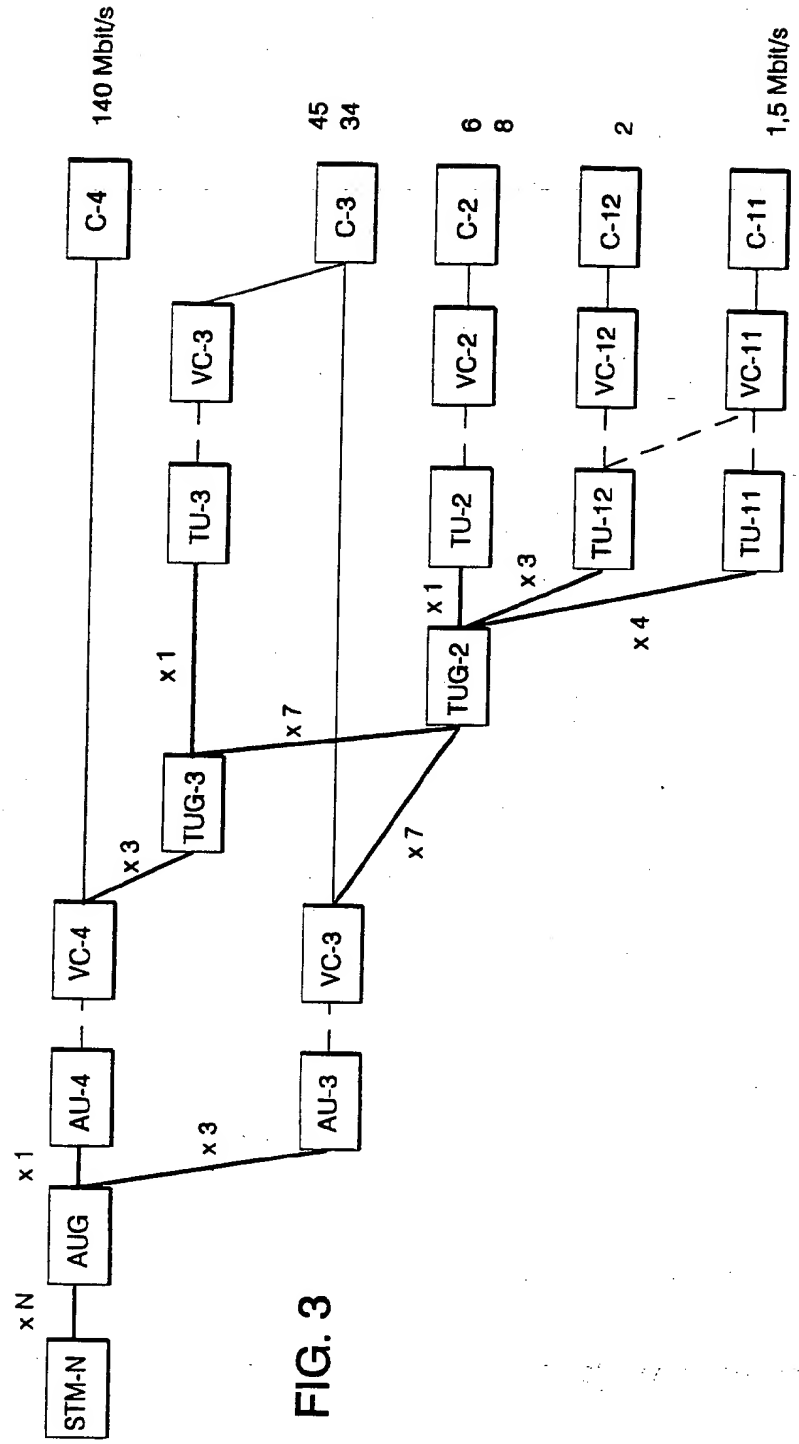


FIG. 3

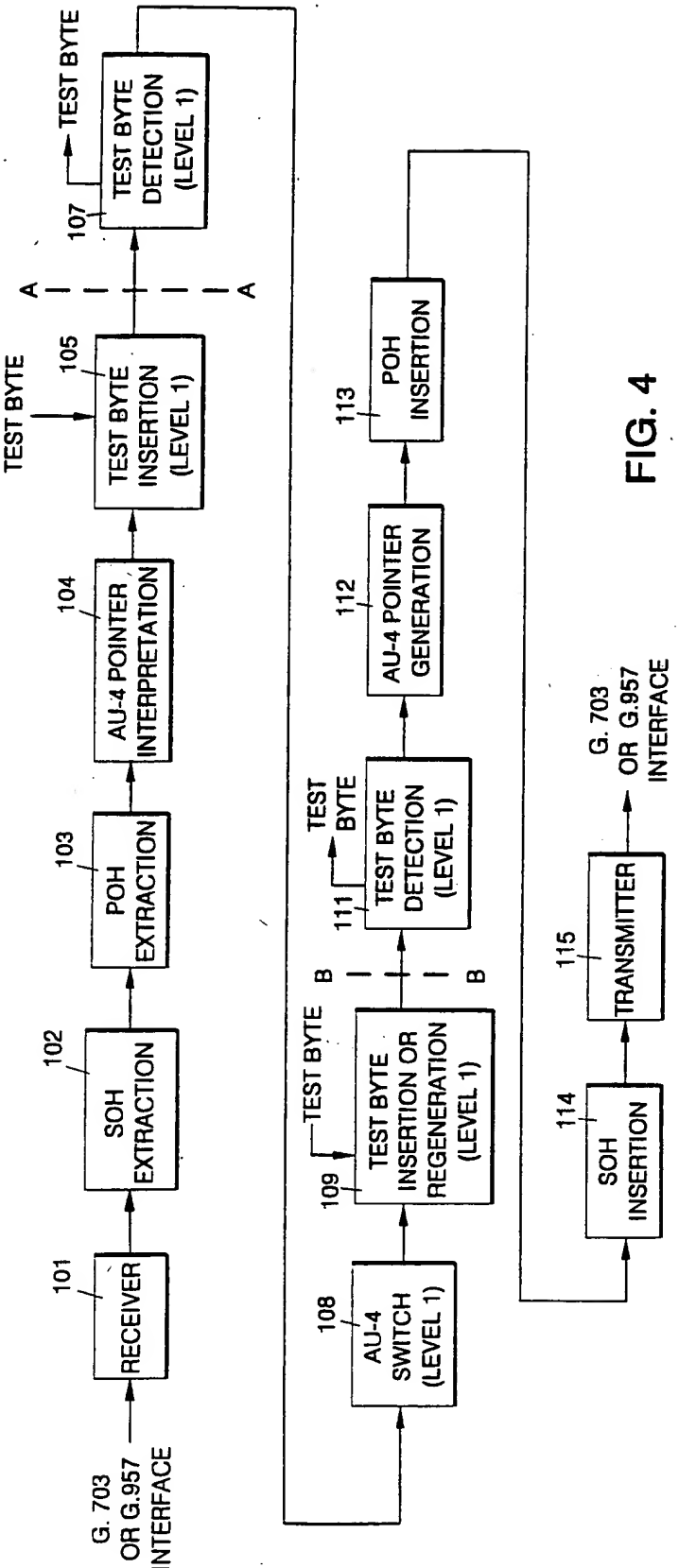


FIG. 4

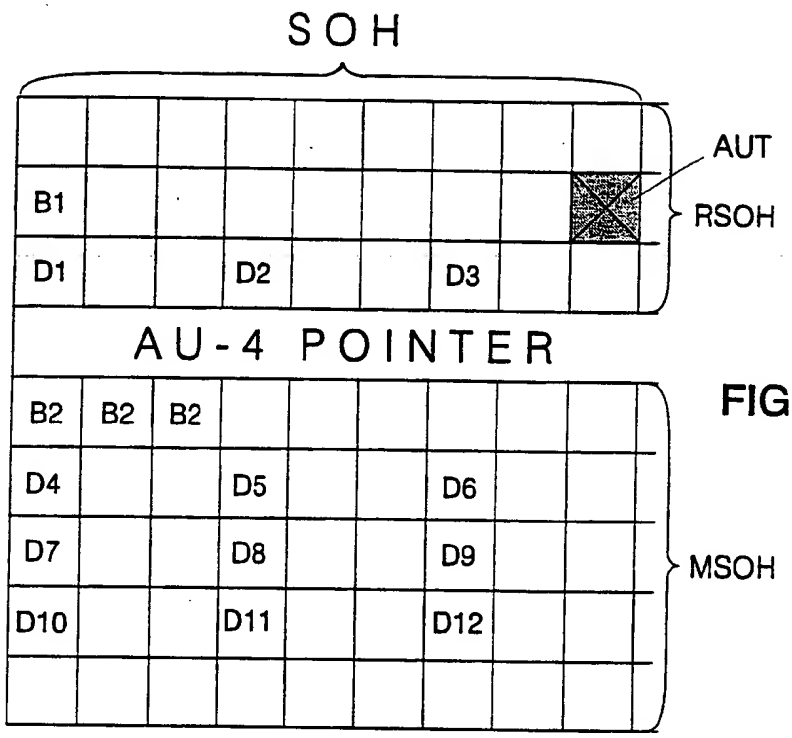

SOH
AUT
RSOH
B1
D1
D2
D3
AU-4 POINTER
B2
B2
B2
D4
D5
D6
D7
D8
D9
D10
D11
D12
MSOH

FIG. 5

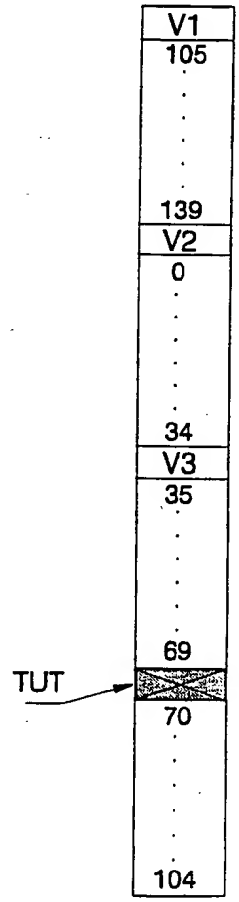

V1
105
139
V2
0
34
V3
35
69
TUT
70
104

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 93/00519

A. CLASSIFICATION OF SUBJECT MATTER

IPC5: H04J 3/14, H04L 12/26
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC5: H04B, H04J, H04L, H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

ORBIT: WPAT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP, A1, 0344534 (SIEMENS AKTIENGESELLSCHAFT), 6 December 1989 (06.12.89), column 2, line 14 - column 3, line 25, figures 1-3, claims 1-2, abstract --	1-10
P,X	US, A, 5251204 (NAOYUKI IZAWA ET AL), 5 October 1993 (05.10.93), column 4, line 27 - line 57, figures 1-4, abstract --	1-10
&,X	JP, A, 4127743 (FUJITSU LIMITED), 28 April 1992 (28.04.92) --	1-10

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" erlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 March 1994	15 -03- 1994
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Magnus Stiebe Telephone No. +46 8 782 25 00

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 93/00519

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Patent Abstracts of Japan, Vol 16,No 18, E-1155, abstract of JP, A, 3-235599 (NEC CORP), 21 October 1991 (21.10.91) --	1-10
X	Patent Abstracts of Japan, Vol 13,No 144, E-740, abstract of JP, A, 63-306725 (NEC CORP), 14 December 1988 (14.12.88) --	1-10
A	EP, A2, 503486 (STANDARD ELEKTRIK LORENZ), 16 Sept 1992 (16.09.92), claims 1-11 --	1,10

INTERNATIONAL SEARCH REPORT

Information on patent family members

28/01/94

International application No.
PCT/FI 93/00519

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A1- 0344534	06/12/89	SE-T3- 0344534	
		AU-B- 590489	02/11/89
		JP-A- 2026428	29/01/90
		US-A- 4964112	16/10/90
US-A- 5251204	05/10/93	JP-A- 4127743	28/04/92
JP-A- 4127743	28/04/92	US-A- 5251204	05/10/93
EP-A2- 503486	16/09/92	NONE	